The New Generation of SKYPLEX Multi Carrier Demultiplexer Demodulator ASIC

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ABSTRACT

The most important feature of SKYPLEX system is the capability to offer uplink data rates from 2 Mbps up to 7.3 Mbps, both in TDMA and SCPC. The satellite On-Board signal processing section is in charge of demodulating and multiplexing several of these asynchronous uplink data flows in a single data stream at 55 Mbps fully compatible with the DVB-S standard.
This paper presents the functionality and performance of the third generation On-Board ASIC, implementing a digital Multi Carrier Demultiplexer and Demodulator (MCDD) for the new SKYPLEX programs. The second generation of SKYPLEX MCDD (operating on Hot Bird™ 5 satellite) was suitable for either single high rate or triple low rate multiple QPSK continuous (SCPC) and TDMA mode carriers. Any combination of low rate carriers (~2 Mbps) is permissible and the carriers are independent and asynchronous to each other. Presently, the operational working point of the Skyplex Unit in terms of Eb/N0 is about 11 dB.
The third generation of SKYPLEX will provide commercial DVB compliant services, i.e. DTH DTV, Internet 'Push' and multimedia applications, within the Hot Bird™ 6 coverage area. They shall also support data transmission, and more complex traffic routing policies. The goal is to minimise the uplink station RF power and the ground antenna size. A reduced complexity and hence lower cost for the TDMA network implementation is the main objective for the effective utilisation of the SKYPLEX system for thousands of users.
These stringent requirements have been satisfied by including DVB-RCS MPEG Packet Turbo Coding FECs in the uplink (R=4/5 and 6/7). The new Eb/N0 working range is between 6 – 7 dB. This new value for the Eb/N0 creates a severe operational environment for correct carrier demodulation and TDMA operation, hence a more complex design for the MCDD implementation.

INTRODUCTION

The demodulator ASIC receives a high rate carrier at an Intermediate Frequency (IF) equal to ¼ of the sampling rate. After the anti-aliasing filter, a single ADC samples the input signal at a fixed sampling rate of 14.66 MHz. Each high rate carrier is then processed in continuous or TDMA mode.
In the case of low rate carriers, an input polyphase filter is activated to simultaneously frequency demultiplex the three low rate carriers, which are 1.833 MHz frequency spaced. These carriers occupy the same bandwidth of a single high rate carrier. The three channels are simultaneously and independently processed by the MCDD, which provides three output data streams.
The input carrier frequency and power unbalance specifications are severe and require specific attention, especially in TDMA mode.
A new Start of Burst detector circuit has been simulated and implemented and both timing and carrier recovery have been re-designed. The large frequency unbalances (8% of symbol rate) and cycle slipping issues (cycle slip probability $<10^{-8}$) made every feed forward synchronisation scheme practically unfeasible.
Keeping in mind that the demodulator should work both in TDMA and SCPC mode, a good trade-off has been found by investigating mixed feed forward and feedback recovery schemes. This demodulator architecture has the advantage in both acquisition time (due to the feed forward starting estimate at the beginning of each burst) and tracking performances (due to the feedback loops). The main references for the DSP algorithms are reported at the end of the article.
The data rates at which the demodulator is able to operate range from slightly more than 2 Mbps up to 8 Mbps with implementation loss lower than 1 dB. All configurations may be changed on-the-fly and the signal processing parameters may be tuned during the mission.

A great versatility has been added by allowing fully programmable packet and burst length in a symbol by symbol basis. This will guarantee that the demodulator will be able to operate with other frame formats. Moreover other ancillary circuits have been added i.e. packet synchronisation and special packet identification.

FUNCTIONAL BLOCK DIAGRAM

The overall block diagram is depicted in the Fig. 1.

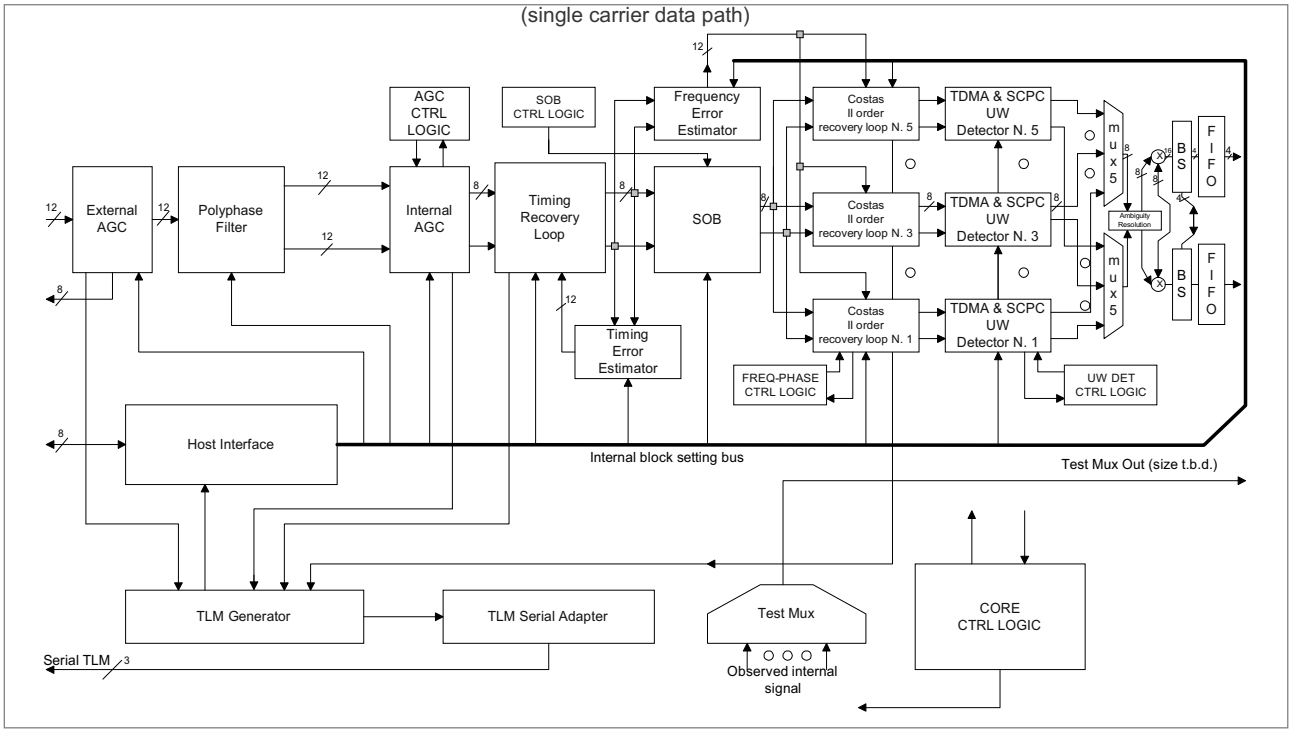

Fig. 1 MCDD Functional Block Diagram

The Fig.1 shows the processing path for a single carrier. The DSP resources in case of multicarrier operation are used in timesharing. Several Finite State Machines (FSM) implement the control logic networks for the correct operation of the MCDD in all operational modes. The ASIC is equipped with 230 byte registers for the MCDD configuration and 19 registers for telemetry purpose. For testing and tuning activity a parallel test multiplexer (150 bits wide) has been included to have a large internal signal visibility.

POLYPHASE FILTER

A simple multiplication-free downmux is used in high rate mode for baseband down conversion due to the fact that the Intermediate Frequency (IF) is equal to ¼ of the sampling rate.
Due to channel spacing, the processing for the three low rate carriers for channel frequency demultiplexing, I-Q baseband down conversion and sampling decimation by four is accomplished through a polyphase filter structure as shown in. Fig. 2
The FIR prototype filter has an impulse response of 48 taps. The input data samples are 12 bits wide. The polyphase filter is implemented around 6 combinatorial multipliers. The FFT is a serial implementation using shifters and adders. All of the filter coefficients are programmable in order to optimise the cascade frequency response of the frequency channels multiplexing and the single channel raised cosine filtering to minimise inter-symbol and cochannel interference.

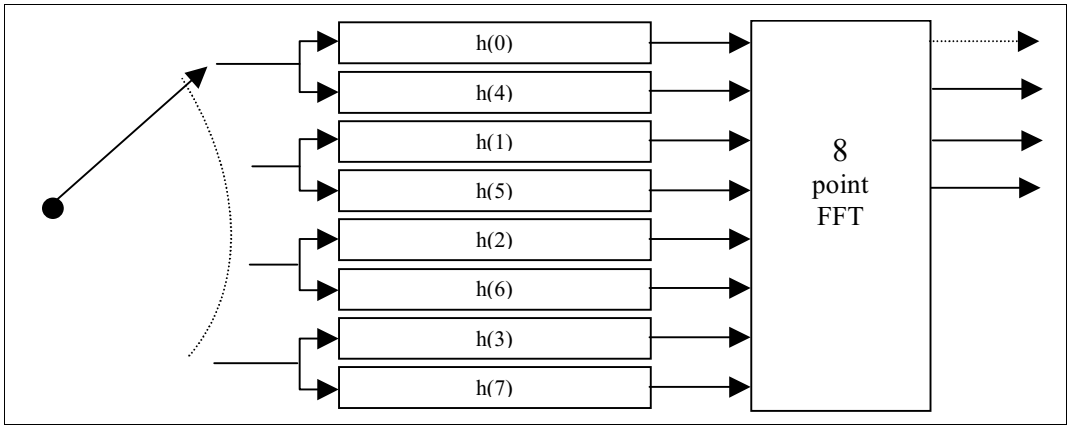

Fig. 2 Low Rate Carrier Frequency Demultiplexing Block Diagram

AUTOMATIC GAIN CONTROL (AGC) CIRCUITS

Two AGCs are provided. The external one is the digital part of an AGC loop to control the gain of the analog front end in a closed or open loop configuration. The generic AGC algorithm block diagram is depicted in Fig. 3.
The carrier AGC is an all digital loop that is used to adjust and track the correct signal dynamic. Moreover, the loop can be programmed with different bandwidths and fixed gains during guard time to ensure the correct burst acquisition and signal tracking during burst demodulation.

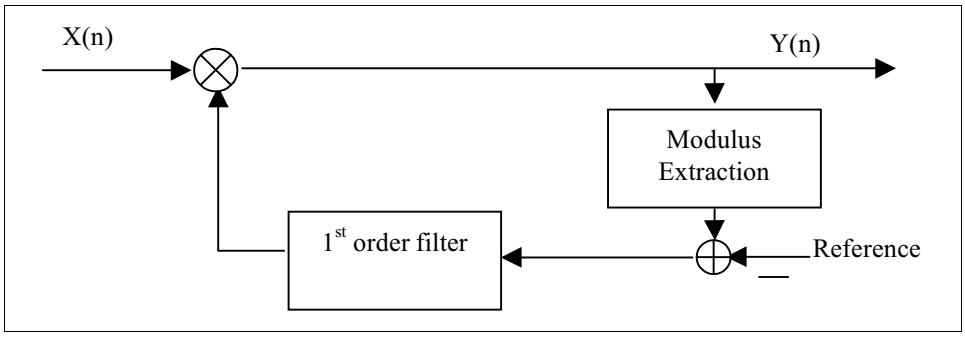

Fig. 3 AGC loops block diagram

The modulus extraction is made through the well-known approximation:

$$m = \max(\text{abs}(I), \text{abs}(Q)) + 0.375 * (\min(\text{abs}(I), \text{abs}(Q))) \quad (1)$$

INTERPOLATOR FILTER AND TIMING RECOVERY LOOP

Fig. 4 shows a simplified block diagram of the symbol synchroniser and SRRC filtering loop.
The implemented symbol synchroniser is based upon the well-known timing error detector proposed by Gardner in [1]. It requires two samples per symbol and operates equally well in SCPC and/or TDMA mode. The detector algorithm is described by the equation:

$$\varepsilon_k = I_k * (I_{k+1/2} - I_{k-1/2}) + Q_k * (Q_{k+1/2} - Q_{k-1/2}) \quad (2)$$

where k is the symbol number. The values of the pair of symbols lying between the $(k-1)^{th}$ and k^{th} strobes are $I_{k-1/2}$, $Q_{k-1/2}$. An error sample ε_k is generated for each symbol. A data aided initial timing estimation is used in TDMA mode. The timing estimation value is fed into the interpolator to force the loop to start from a quasi-optimum working point to speed up the steady state acquisition and to avoid possible loop hang-up.
It is proven in [1] that the ε_k is independent of the carrier phase offset. Therefore, the timing loop can lock prior to locking of the carrier phase acquisition. However, the timing loop performance is sensitive to frequency offset. It is demonstrated that timing loop works well with a frequency offset in the range of 8-10% of the symbol rate. Thus no frequency correction is performed prior to the timing loop.

The digital interpolator and the Squared Root Raised Cosine (SRRC) filter are implemented and optimised as a single filter. Sixteen phase responses are used with 20 taps. 8 different sets of impulse response are hardwired to accommodate the possible different symbol rates. The error detector signal ε_k is applied to a first order loop with time variable bandwidth. Three constant loop values are used in order to enhance the loop acquisition performance and to maintain the steady state timing error variance low.

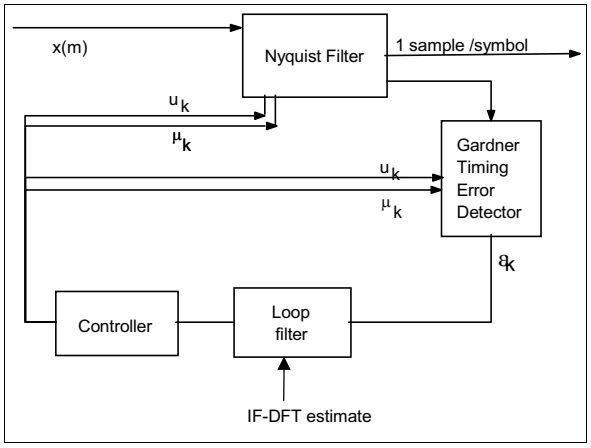

Fig. 4 Simplified Block Diagram of the Symbol Synchronizer

FEED FORWARD TIMING ERROR ESTIMATE

Timing Error estimate is based on 4-point FFT algorithm. This data aided algorithm works during the burst preamble where a sequence of 0-0-π-π preamble is present. This sequence produces a sinusoid of period 4*Ts (Ts is the symbol duration). The timing estimation is based on the calculation of the phase of this sinusoid. The original signal can have non-zero frequency error. The input signal is decimated by two and a new value for timing estimate is computed every 4 input samples. This result is an overall decimation of 8-samples i.e. there is a new value for timing estimation every 8 samples. Fig. 5 represents a sketch of the algorithm.

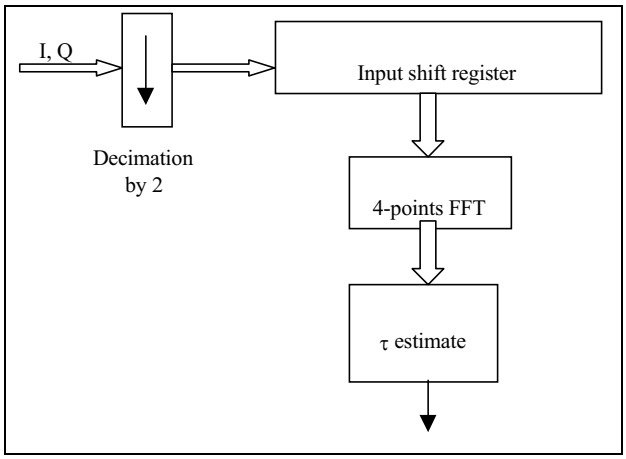

Fig. 5 Feed Forward Timing Estimation

4-point FFT is computed each 4 (decimated) input samples. Punctual estimation of τ (timing error) is performed by the equation:

$$\hat{\tau} = \frac{1}{2}\arg\left(P_{\frac{N}{4}} P^{*}_{\frac{3N}{4}} \right) \tag{3}$$

the symbol * represents the complex conjugate operator. The $P_{\frac{N}{4}}$ and $P^{*}_{\frac{3N}{4}}$ are bin 1 and conjugate of bin 3 of 4-point FFT respectively. To reach a more accurate timing estimation, an average is performed over a programmable number of FFT estimation.
The *arg()* function has been implemented with a CORDIC algorithm.

START OF BURST DETECTOR

The Start of Burst Detector (SoB) is used in TDMA mode to detect the preamble of the burst and trigger the complete signal acquisition prior the Unique word (UW) detection and the final burst demodulation.
An FFT Power Detector and Detection Logic implement the SoB circuit. The FFT Power Detector estimates input signal and noise power. The Detection Logic compares signal power respect to the noise power detecting the start of a valid burst. The signal dynamic does not influence the probability of burst detection due to the inherent differential characteristic of the designed algorithm. The SoB architecture is represented in Fig. 6.

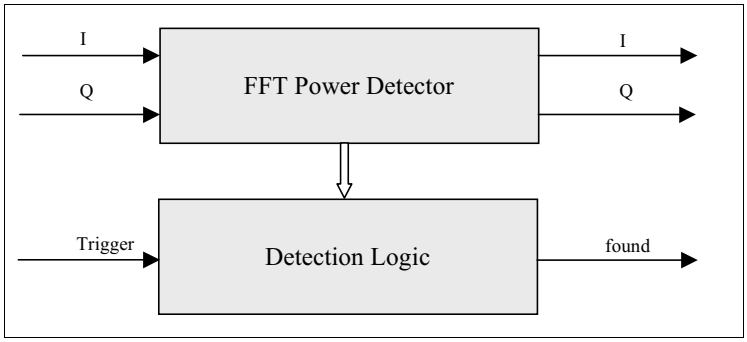

Fig. 6 Start of Burst Detector Architecture

The FFT input shift register is used as a delay buffer to feed the phase recovery loops with I and Q filtered samples. Burst preamble has a 0-0-π–π sequence sampled at two samples per symbol. Input to FFT stage is taken every 8 samples from the input shift registers. With such tapping the FFT is on the same carrier phasor position i.e. a clean carrier. From this structure it can be seen that any preamble having a 4 symbol repetition pattern could be used for Start Of Burst detection purposes.
On each FFT bin is performed a modulus extraction operation using (1). These values are used to compute the signal and noise power values.
The Detection Logic is initialised by the *Trigger* signal generated by the Control Logic. The *found* signal triggers the successive steps for the complete burst acquisition.

FEED FORWARD FREQUENCY ERROR ESTIMATE

Given the 0-0-π-π preamble sequence, a reliable frequency estimate may be obtained with the structure depicted in the Fig. 9. This Data Aided phase increment-based estimator, for wide frequency estimation ranges, is also capable of operating without timing information.

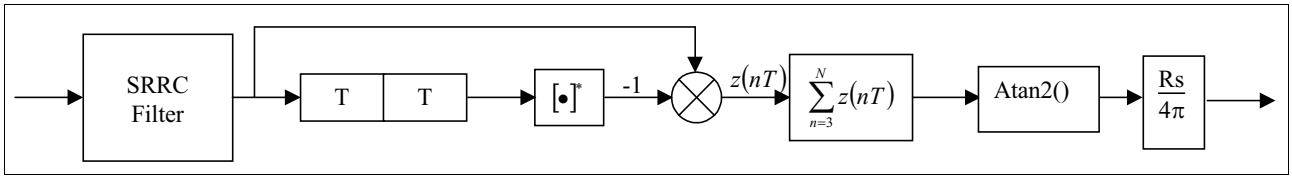

Fig. 7 Feed Forward Frequency Estimator

Given the signal $x(n) = Ae^{j\phi_c} e^{j2\pi\Delta f T_s n} \sin\left(\frac{\pi}{2} n + \tau\right)$ it's easy to see that an estimate of the frequency error Δf is equal to $\hat{f} = \text{atan2}\left\{\sum_{n}^{N} \left(x(n) * \left(-x(n-2)^*\right)\right)\right\} \frac{R_s}{4\pi}$. The symbol * which follows a quantity represents the complex conjugate operator. The Atan2 operation is performed with a CORDIC algorithm.

PHASE AND FREQUENCY RECOVERY LOOPS

Phase and Frequency Recovery are made through a bank of 5 recovery loops. The well-known COSTAS LOOP is used as recovery scheme. All blocks are equal, the only difference being the programmed start up centre frequency. Fig. 8 depicts a single COSTAS Loop block diagram.

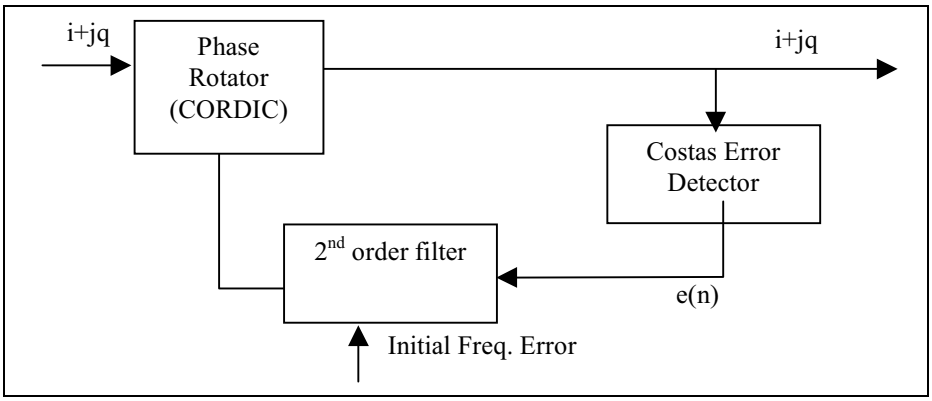

Fig. 8 COSTAS Loop Block Diagram

The operation of the recovery loop banks depends on the different acquisition strategy for SCPC or TDMA modes.
The TDMA acquisition uses the frequency estimate f_{ext} obtained with the frequency estimation algorithm. In order to cope with the variance of such an estimation, the five COSTAS are preloaded with f_{ext}, $f_{ext}+\Delta f$, $f_{ext}-\Delta f$, $f_{ext}+2\Delta f$, $f_{ext}-2\Delta f$ where the Δf are properly programmed depending on the pull-in range of the loops.
Each COSTAS feeds a UW detector. When one detector finds the UW, the relative COSTAS output survives. In case of multiple detection the path that survives is the one nearest to f_{ext}.
In SCPC acquisition the five COSTAS are preloaded with 0, Δf, -Δf, 2Δf, -2Δf where the Δf are properly programmed depending on the pull-in range of the loops to cover the maximum frequency error range. Each COSTAS feeds a MPEG header detector and the packet synchronisation FSM. When one FSM finds the correct packet synchronisation, the relative COSTAS output survives. In case of multiple detection the path that survives is the one nearest to the zero frequency error offset.

ANCILLARY CIRCUIT

The MCDD is equipped with others ancillary circuits:
- ⇒ Fully programmable UW or MPEG packet synchronisation FSMs;
- ⇒ Programmable PID recognition for short burst detection in TDMA Reed Solomon Mode;
- ⇒ Serial and Parallel TLM generation to monitor the internal status of the MCDD;
- ⇒ Programmable Soft quantisation Symbols Output dynamic adjustments to correctly tune the 4 bit soft quantised demodulated symbols to reach the optimum performance of the Turbo Soft Decoding process.

PERFORMANCES

The MCDD and Turbo Decoder ASICs have been integrated in SKYPLEX for Hot Bird™ 6 as shown in Fig. 9.
The performances in all configurations are inside the specification. The degradation of the Eb/N0 in terms of BER for worst-case signal conditions is below 1 dB and the burst loss is less than 1 burst lost per hour. The system test and tuning phase have been completed on EM SKYPLEX model. Flight modules are presently under construction.

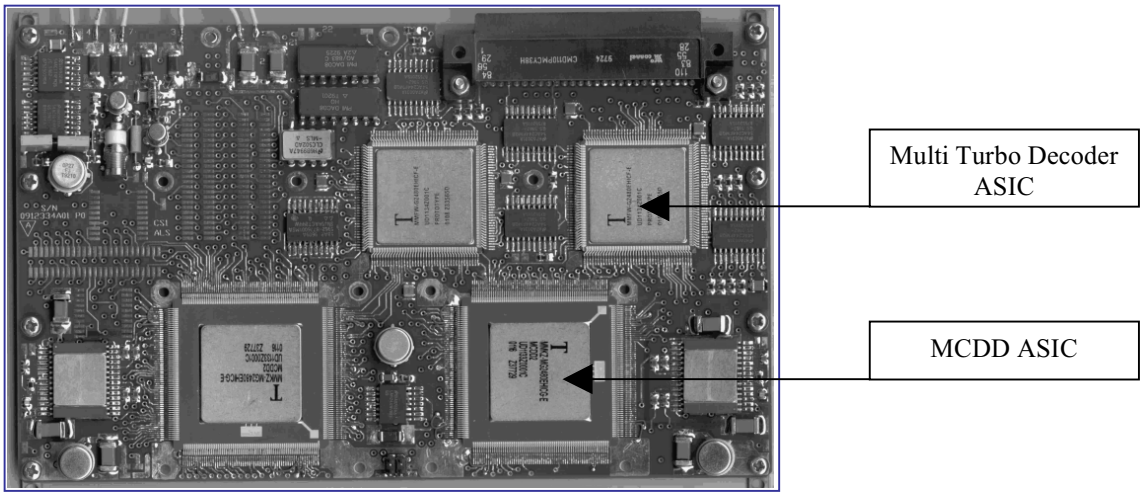

Fig. 9 Twin Demodulator & Turbo decoder Board

ASIC IMPLEMENTATION AND COMPLEXITY

- Technology utilised: ATMEL MG2RT Radiation Tolerant 0.5-Micron Sea of Gates 3 metal layers.
- Matrix utilised: MG2480E (480 Kgates usable 360K).
- Package: MQFP 256 pins.
- Measured power consumption: 0.8 – 1.2 Watt depending on operational configuration (core at 3.3 V and system clock 29.3 MHz).
- DSP algorithms developed in fixed point C++ and matched to the VHDL-RTL models.
- ASIC synthesis: SYNOPSYS Design Compiler 1999.10-4.
- Design Simulation and matching: MODELSIM 5.4c SE.

Table 1 summarises the design complexity for the main blocks previously mentioned.

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Table 1. MCDD ASIC Synthesised Gates Count

Functional Blocks	Total K-Gates
External and Carrier AGC	12
Polyphase Filter and Downmux	28
SRCC Interpolator Filter and Timing loop	53
Start of Burst Detection	55
Feed Forward Timing Estimator	24
Feed Forward Frequency Error Estimator	15
COSTAS Loop Bank	72
UW and Header Detection	46
Output Interface Logic	9
Control Logic and FSMs	19
Microcontroller I/F and Registers	5
Serial and parallel TLM	3
Testing Multiplexer	3
Buffering and Clock Tree	4
Total ASIC gate Count	**348**
MG2 Matrix utilisation Factor	**79 %**

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